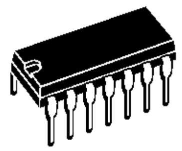
SGS-THOMSON MICROELECTRONICS

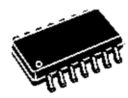
TS3V902

3V INPUT/OUTPUT RAIL TO RAIL DUAL CMOS OPERATIONAL AMPLIFIER (WITH STANDBY POSITION)

- DEDICATED TO **3.3V** OR **BATTERY SUPPLY** (specified at 3V and 5V)
- RAIL TO RAIL INPUT AND OUTPUT VOLTAGE RANGES
- **STANDBY** POSITION : REDUCED **CONSUMPTION (1µA)** AND **HIGH IMPEDANCE OUTPUTS**
- SINGLE (OR DUAL) SUPPLY OPERATION FROM **2.7V TO 16V**
- EXTREMELY LOW INPUT BIAS CURRENT : **1pA** TYP
- LOW INPUT OFFSET VOLTAGE : **1.5mV max.**
- SPECIFIED FOR **600Ω** AND **100Ω** LOADS
- LOW SUPPLY CURRENT : 200µA/Ampli



N
DIP14
(Plastic Package)

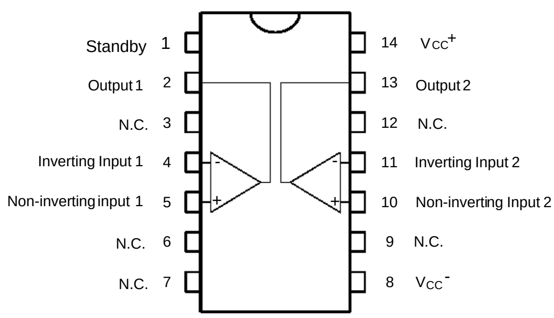


D
SO14
(Plastic Micropackage)

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TS3V902I/AI/BI	-40, +125°C	•	•

PIN CONNECTIONS (top view)



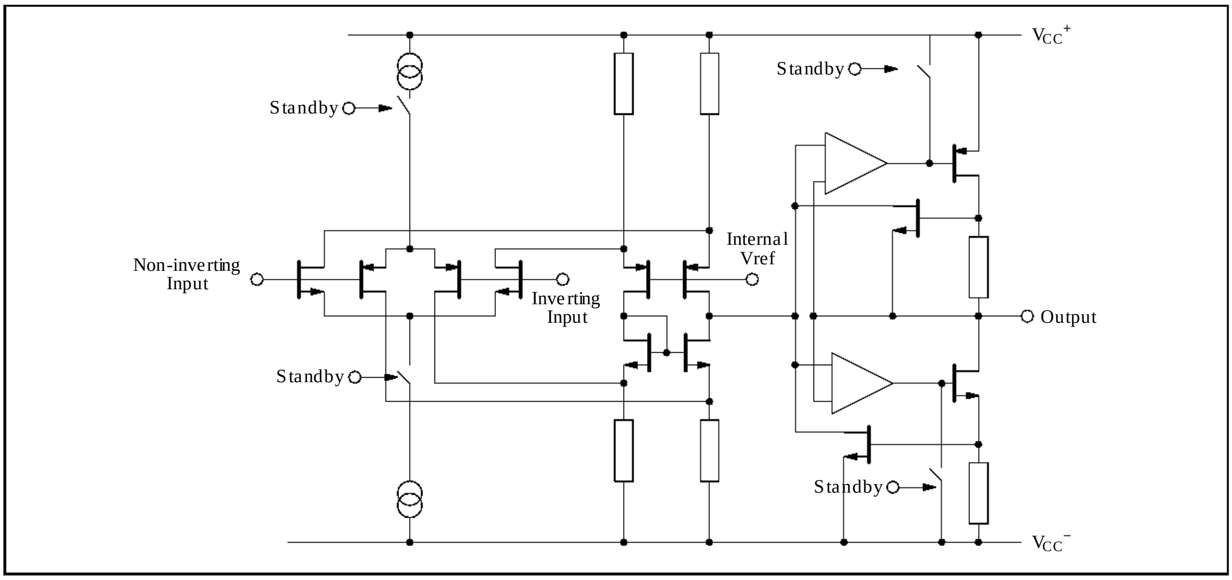
DESCRIPTION

The TS3V902 is a RAIL TO RAIL dual CMOS operational amplifier designed to operate with single or dual supply voltage.
The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^-.
The output reaches :

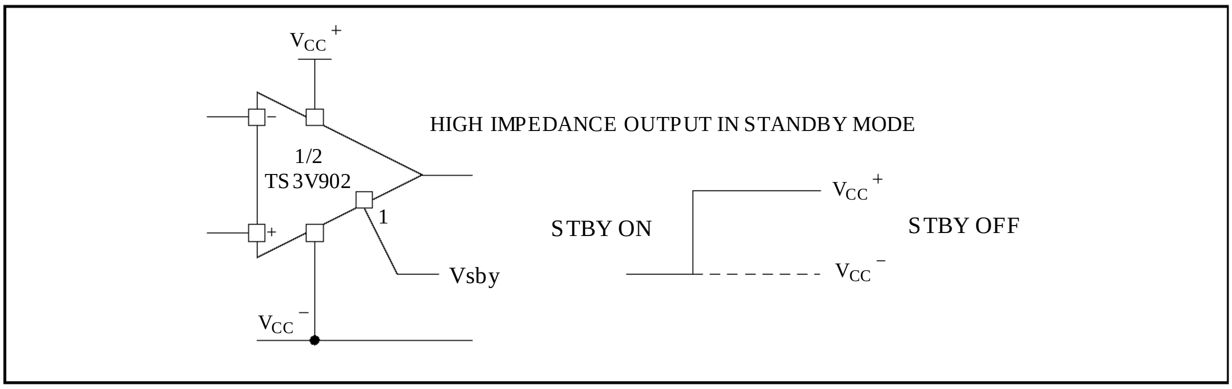
- V_{CC}^- +50mV V_{CC}^+ -50mV   with R_L = 10kΩ
- V_{CC}^- +350mV V_{CC}^+ -350mV   with R_L = 600Ω

This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 200µA/amp. (V_{CC} = 3V).
Source and sink output current capability is typically 40mA (at V_{CC} = 3V), fixed by an internal limitation circuit.
The TS3V902 can be put on STANDBY position (only 0.5µA and high impedance outputs).

SCHEMATIC DIAGRAM (1/2 TS3V902)



STANDBY POSITION



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage - (note 1)	18	V
V_{id}	Differential Input Voltage - (note 2)	±18	V
V_i	Input Voltage - (note 3)	-0.3 to 18	V
I_{in}	Current on Inputs	±50	mA
I_o	Current on Outputs	±130	mA
T_{oper}	Operating Free Air Temperature Range TS3V902I/AI/BI	-40 to +125	^oC
T_{stg}	Storage Temperature	-65 to +150	^oC

Notes :
1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3V.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.7 to 16	V
V_{icm}	Common Mode Input Voltage Range	V_{CC}^- -0.2 to V_{CC}^+ +0.2	V

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, R_L,C_L connected to $V_{CC}/2$, Standby OFF, $T_{amb} = 25^oC$ (unless otherwise specified)

Symbol	Parameter		TS3V902I/AI/BI			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($V_{ic} = V_o = V_{CC}/2$) $T_{min.} \leq T_{amb} \leq T_{max.}$	TS3V902 TS3V902A TS3V902B TS3V902 TS3V902A TS3V902B			12 5 1.5 12 7 3	mV
DV_{io}	Input Offset Voltage Drift			5		µV/°C
I_{io}	Input Offset Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$			1	100 200	pA
I_{ib}	Input Bias Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$			1	150 300	pA
I_{CC}	Supply Current (per amplifier, $A_{VCL} = 1$, no load) $T_{min.} \leq T_{amb} \leq T_{max.}$			200	300 400	µA
CMR	Common Mode Rejection Ratio $V_{ic} = 0$ to 3V, $V_o = 1.5V$			60		dB
SVR	Supply Voltage Rejection Ratio ($V_{CC}^+ = 2.7$ to 3.3V, $V_O = V_{CC}/2$)			80		dB
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_O = 2.5V$ to 7.5V) $T_{min.} \leq T_{amb} \leq T_{max.}$		3 3	10		V/mV
V_{OH}	High Level Output Voltage ($V_{id} = 1V$) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$	2.95 2.9 2.2 2.8 2.1	 2.96 2.6 2		V
V_{OL}	Low Level Output Voltage ($V_{id} = -1V$) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$		 50 350 900	50 100 600 150 900	mV
I_o	Output Short Circuit Current ($V_{id} = \pm 1V$)	Source ($V_o = V_{CC}^-$) Sink ($V_o = V_{CC}^+$)		40 40		mA
GBP	Gain Bandwidth Product ($A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, f = 100kHz)			0.7		MHz
SR	Slew Rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1.3V$ to 1.7V)			0.5		V/µs
∅m	Phase Margin			30		Degrees
e_n	Equivalent Input Noise Voltage ($R_s = 100\Omega$, f = 1kHz)			30		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel Separation (f = 1kHz)			120		dB

STANDBY MODE

$V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, $T_{amb} = 25^oC$ (unless otherwise specified)

Symbol	Parameter	TS902I/AI/BI			Unit
		Min.	Typ.	Max.	
$V_{inSBY/ON}$	Pin 1 Threshold Voltage for STANDBY ON		1.2		V
$V_{inSBY/OFF}$	Pin 1 Threshold Voltage for STANDBY OFF		1.2		V
$I_{CC\ SBY}$	Total Consumption in Standby Position (STANDBY ON)		0.5		µA

ELECTRICAL CHARACTERISTICS

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, R_L,C_L connected to $V_{CC}/2$, Standby OFF, $T_{amb} = 25^oC$ (unless otherwise specified)

Symbol	Parameter		TS3V902I/AI/BI			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($V_{ic} = V_o = V_{CC}/2$) $T_{min.} \leq T_{amb} \leq T_{max.}$	TS3V902 TS3V902A TS3V902B TS3V902 TS3V902A TS3V902B			12 5 1.5 12 7 3	mV
DV_{io}	Input Offset Voltage Drift			5		$\mu V/^oC$
I_{io}	Input Offset Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$			1	100 200	pA
I_{ib}	Input Bias Current - (note 1) $T_{min.} \leq T_{amb} \leq T_{max.}$			1	150 300	pA
I_{CC}	Supply Current (per amplifier, $A_{VCL} = 1$, no load) $T_{min.} \leq T_{amb} \leq T_{max.}$			230	350 450	µA
CMR	Common Mode Rejection Ratio $V_{ic} = 1.5$ to $3.5V$, $V_o = 2.5V$			 85		dB
SVR	Supply Voltage Rejection Ratio ($V_{CC}^+ = 2.7$ to $3.3V$, $V_O = V_{CC}/2$)			80		dB
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_O = 1.5V$ to $3.5V$) $T_{min.} \leq T_{amb} \leq T_{max.}$		7 7	30		V/mV
V_{OH}	High Level Output Voltage ($V_{id} = 1V$) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$	4.95 4.85 4.2 4.8 4.1	 4.9 4.55 3.7		V
V_{OL}	Low Level Output Voltage ($V_{id} = -1V$) $T_{min.} \leq T_{amb} \leq T_{max.}$	$R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$		 50 450 1400	50 100 680 150 900	mV
I_o	Output Short Circuit Current ($V_{id} = \pm 1V$)	Source ($V_o = V_{CC}^-$) Sink ($V_o = V_{CC}^+$)		60 60		mA
GBP	Gain Bandwidth Product ($A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, $f = 100kHz$)			 0.8		MHz
SR	Slew Rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1V$ to $4V$)			0.8		V/µs
∅m	Phase Margin			30		Degrees

STANDBY MODE

$V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $T_{amb} = 25^oC$ (unless otherwise specified)

Symbol	Parameter	TS902I/AI/BI			Unit
		Min.	Typ.	Max.	
$V_{inSBY/ON}$	Pin 1 Threshold Voltage for STANDBY ON		5.2		V
$V_{inSBY/OFF}$	Pin 1 Threshold Voltage for STANDBY OFF		5.2		V
$I_{CC\ SBY}$	Total Consumption in Standby Position (STANDBY ON)		0.5		µA

TYPICAL CHARACTERISTICS

Figure 1a : Supply Current (each amplifier) versus Supply Voltage

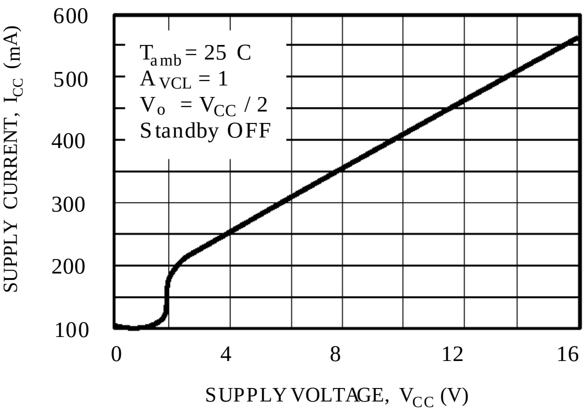


Figure 1b : Supply Current (each amplifier) versus Supply Voltage (in STANDBY)

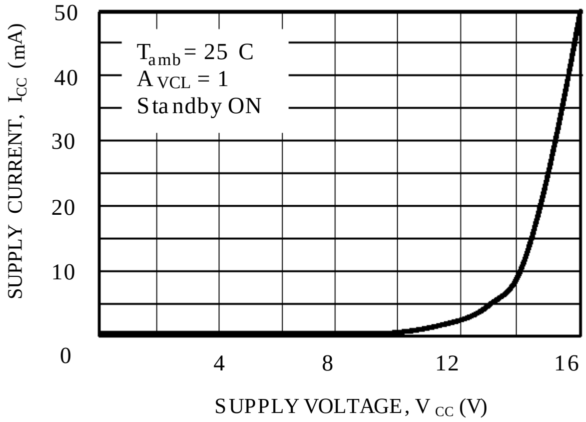


Figure 2 : Input Bias Current versus Temperature

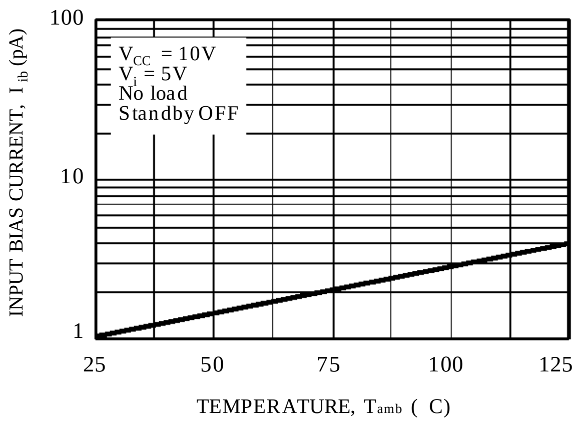


Figure 3a : High Level Output Voltage versus High Level Output Current

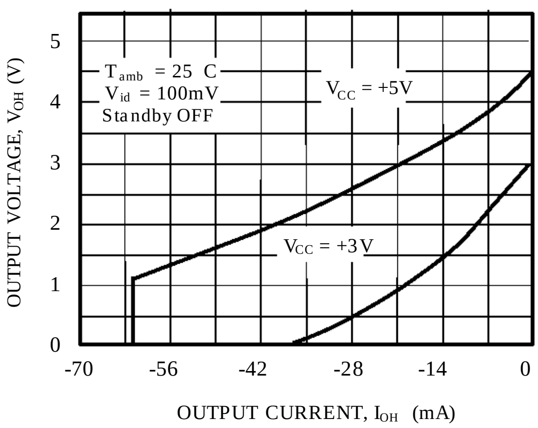


Figure 3b : High Level Output Voltage versus High Level Output Current

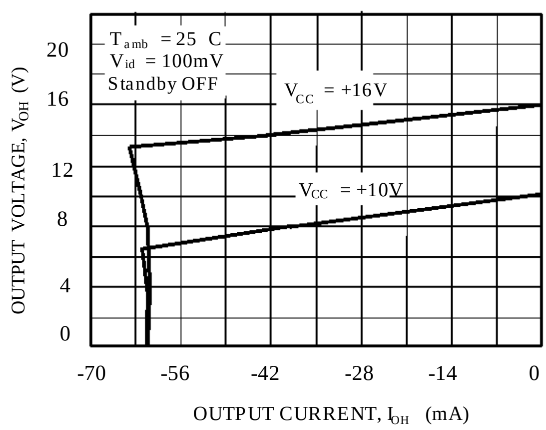


Figure 4a : Low Level Output Voltage versus Low Level Output Current

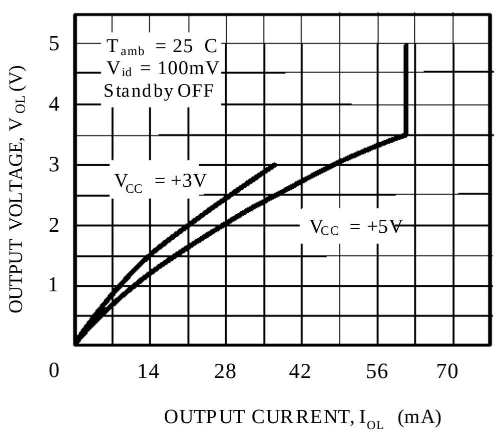


Figure 4b : Low Level Output Voltage versus Low Level Output Current

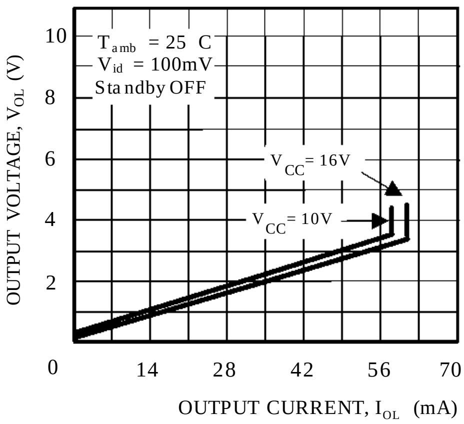


Figure 5a : Open Loop Frequency Response and Phase Shift

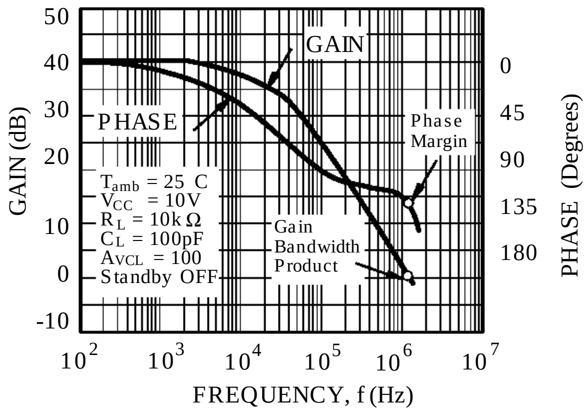


Figure 5b : Open Loop Frequency Response and Phase Shift

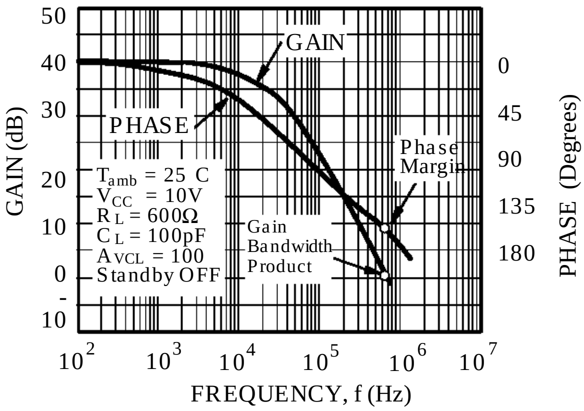


Figure 6a : Gain Bandwidth Product versus Supply Voltage

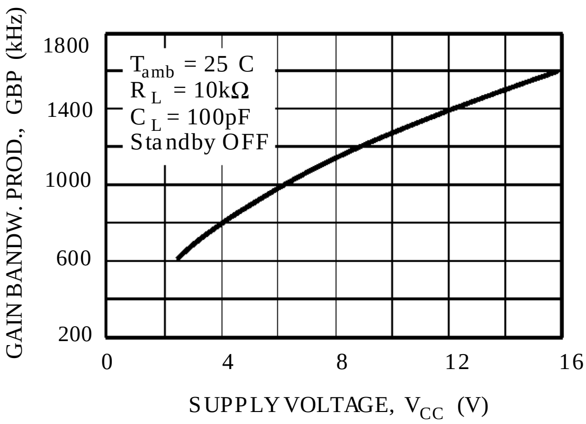


Figure 6b : Gain bandwidth Product versus Supply Voltage

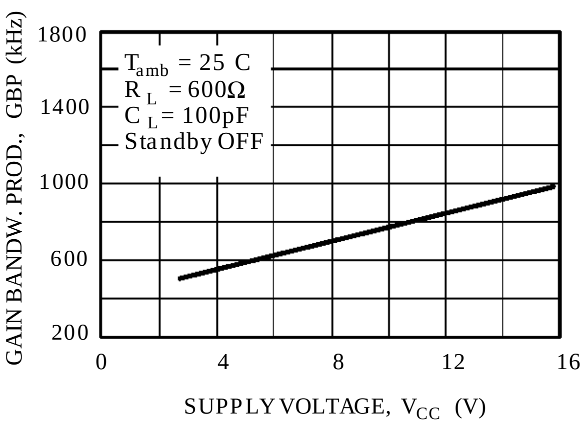


Figure 7a : Phase Margin versus Supply Voltage

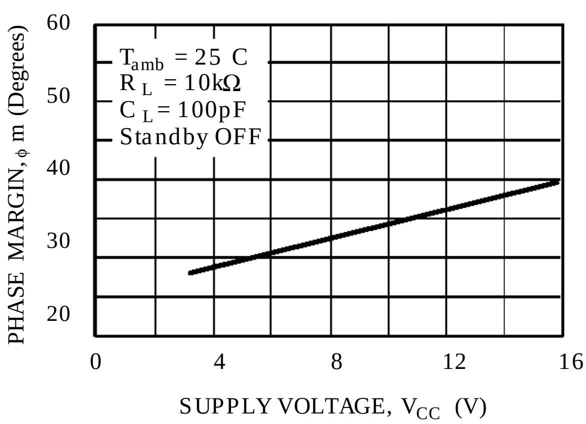


Figure 7b : Phase Margin versus Supply Voltage

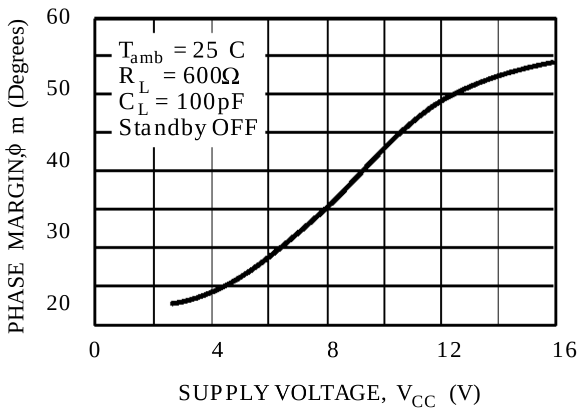
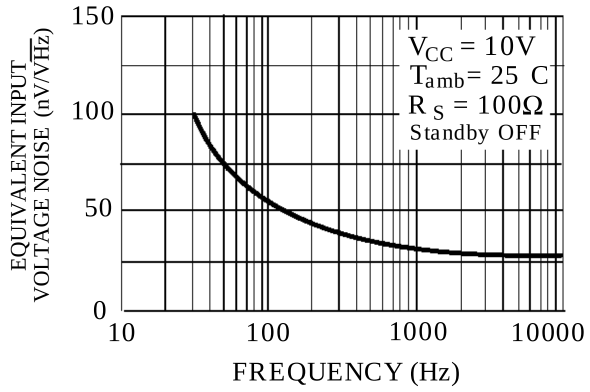


Figure 8 : Input Voltage Noise versus Frequency



STANDBY APPLICATION

The two operators of the TS3V902 are **both** put on **STANDBY.**

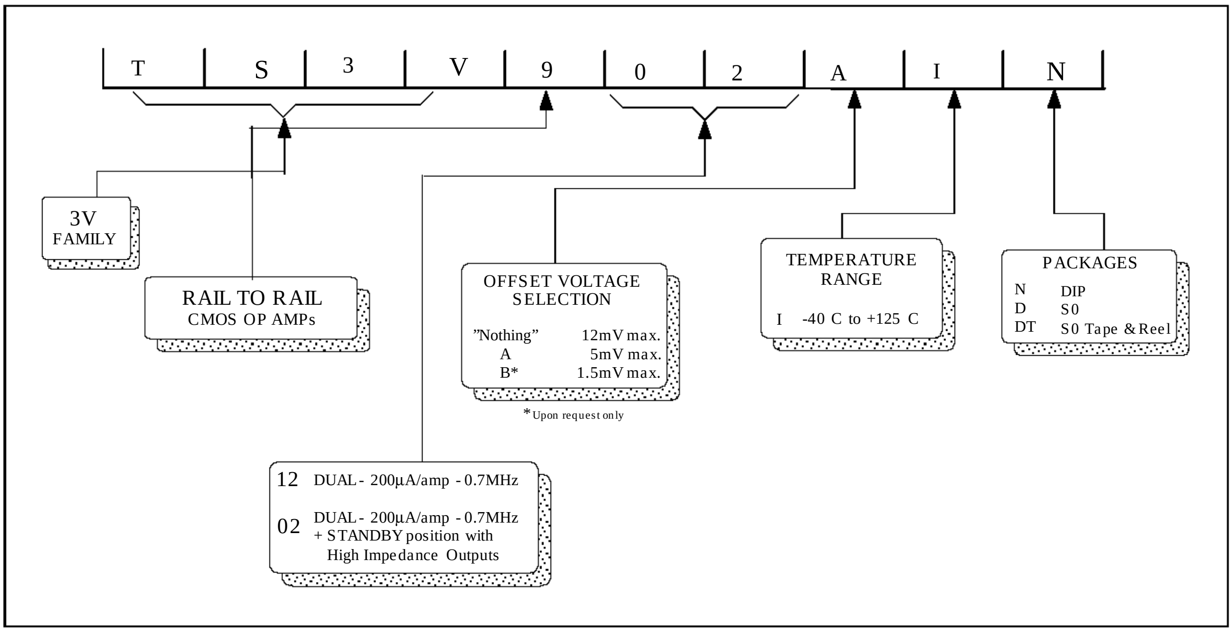
In this configuration (standby ON) :

- The **total consumption** of the circuit is considerably **reduced** down to **0.5µA** (V_{CC} = 3V). This standby consumption versus V_{CC} curve is given figure 1b.
- The **both outputs** are in **high impedance** state. No output current can then be sourced or sinked by the device.

The standby pin 1 should never stay unconnected.

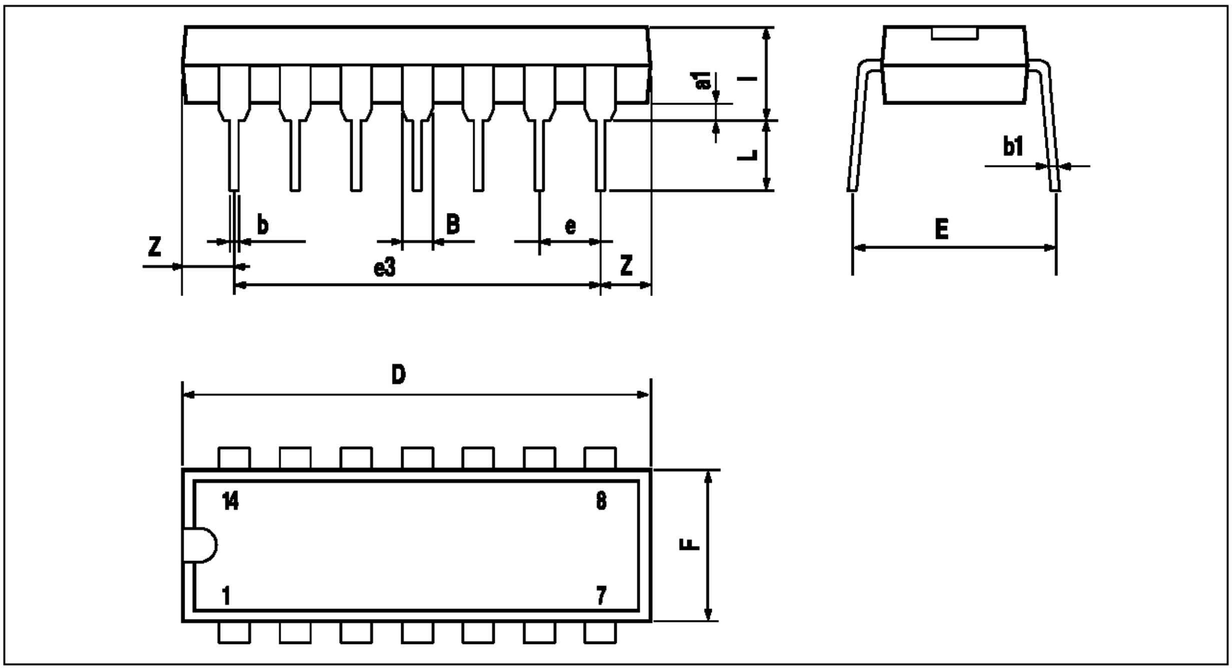
- The **"standby OFF"** state, is reached when the pin 1 voltage is **higher than $V_{in\ SBY/OFF}$.**
- The **"standby ON"** state is assured by a pin 1 voltage **lower than $V_{in\ SBY/ON}$.** (see electrical characteristics)

ORDERING INFORMATION



PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP



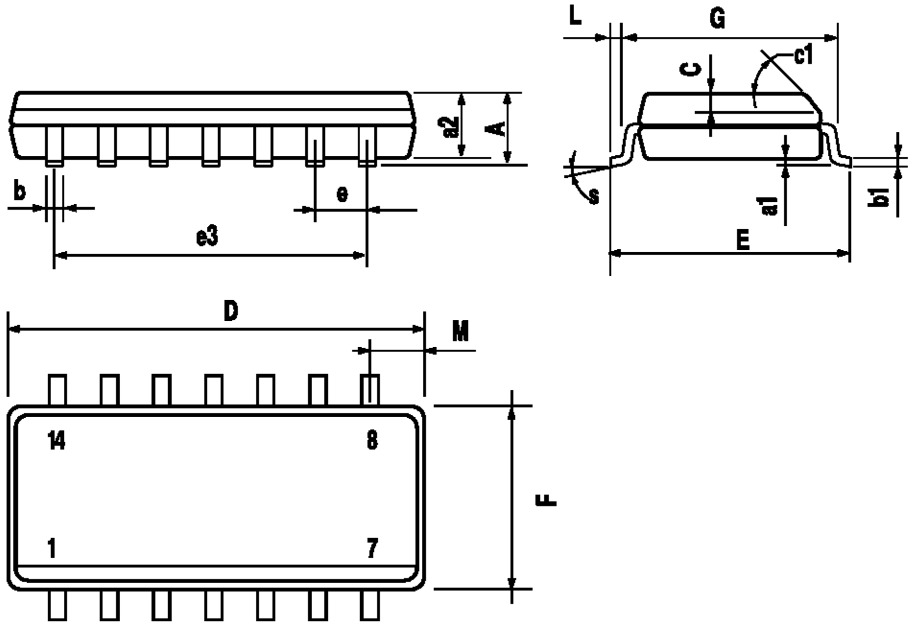
PM-DIP14.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

DIP14.TBL

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO14.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.334
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

SO14.TBL

ORDER CODE :